THE IMPACT OF GATE LENGTH, OXIDE DIELECTRIC MATERIALS, AND OXIDE THICKNESS ON THE GANNT MOSFETS PERFORMANCE.

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Abstract
The expansion of the integrated circuit industry in recent years has been primarily propelled by the progressive growth of metal-oxide-semiconductor field effect transistors (MOSFETs). The device is employed as a rapid switch in computers advanced. The switching speed of MOSFETs is significantly influenced by the selection of gate length, oxide dielectric materials, and oxide thickness. Gallium nitride nanotubes (GaNNT) with remarkable stability in ambient conditions, making them a promising candidate for use as channel material in the forthcoming era of MOSFET technology. This study utilizes ab initio simulation to examine the device functionality of double-gate (DG) GaNNT MOSFETs sub-5 nm under the impact of gate length, oxide dielectric material, and oxide thickness. The findings suggest that enhancing the gate length and dielectric constant, as well as reducing the oxide thickness, can lead to significant improvements in the ratio of \( I_{on}/I_{off} \), subthreshold swing (SS), transconductance (\( g_m \)), power dissipation (PDP), and delay time (\( t \)). The enhancement is notably conspicuous when considering a channel length that is 5 nm for devices of n-type. Hence, GaNNT demonstrates significant potential as a channel material in the advancement of complementary MOSFETs that are compatible with both n-type and p-type devices.

Keywords: density functional theory, field effect transistor, gallium nitride, ab-initio simulations.

Introduction
Silicon (Si) electronic devices have been around for as long as there have been electronics, but scaling-related issues have hampered their advancement [1]. Rapid development in complementary metal-oxide-semiconductor (MOS) technology is based on making transistors smaller while keeping their functionality. With the reduced dimensions of field effect transistors based on Si, the dependableness and efficacy of these FETs are cause for concern. Also, their limitations in scaling and fabrication for leakage current and gate oxide thickness, the emergence of short channels in transistors, such as gate leakage current, and subthreshold swing, further complicate the scaling process [2]. There have been numerous proposals for overcoming these limitations. Nanotubes are another fascinating structure that can further extend the scaling to build MOSFET [3]. One of the benefits of nanotubes for transistors is that they have high carrier mobility [4, 5] since electrical transport in superior nanotubes may be ballistic [6, 7]. A team of researchers from IBM has successfully fabricated a transistor composed of a 9-nm nanotube, demonstrating superior operational efficiency in comparison to other transistors of similar dimensions [8]. In addition to their organic counterparts, nanotubes of non-organic origin can also serve as a viable option for a transistor channel. Several types of nanotubes, such as Boron Nitride nanotube (BN), Gallium Nitride (GaN), Silica, and Nickel Halide, are readily accessible [9]. The focus of our study pertains to GaNNT and their application as channels in transistors. GaN has emerged as a very promising material due to its exceptional properties, making it suitable for numerous applications, such as high power, LED, and high mobility applications. GaN exhibits a distinctive characteristic in the form of a stable hexagonal configuration [10]. GaN bulk transistors have demonstrated exceptional speed, enabling frequencies of up to 205 GHz, hence offering the potential to enhance the speed and cost-effectiveness of existing devices [11]. GaNNT has been observed to possess favorable electrical and optical characteristics, without any compromise on generality. The effective synthesis of single-crystal GaNNT has been achieved through the utilization of the epitaxial casting process [12]. Their uses as devices such as transistors are not well understood. To date, there has been a paucity of studies conducted on the subject matter of GaNNT transistors. In a similar vein to Carbon nanotubes, the utilization of GaNNT can be employed to...
generate field effect transistors. BN nanotubes have been identified as the precursor to GaNNT, and they have been successfully synthesized and demonstrated semiconducting characteristics [13]. Despite belonging to the same class as Nitride nanotubes of III-group, BN and GaN nanotubes exhibit different characteristics [14]. Through the utilization of Density Functional Theory (DFT) principles, simulation investigations have revealed that Boron Nitride and Carbon nanotubes exhibit analogous behaviors.

The primary objective of this investigation is to illustrate the benefits of utilizing GaN material in the design of MOSFETs through the implementation of simulation techniques as per the tenets of DFT. In addition, the study of their relative performance with gate lengths (Lg), dielectric constants, and oxide thicknesses (t oxide) has been carried out in terms of improvement in short-channel effects. For the theoretical analysis of sub-5 nm DGGaNNTMOSFETs- and p-type performance, we employed a quantum-transport ab initio methodology.

**Computational details**

The simulation of transport properties is conducted using the DFT in conjunction with a nonequilibrium Green’s function technique, as applied via the Atomistix Tool Kit [15, 16]. The drain current (Id) at a specific bias/gate voltage (Vd/Vg) is computed using Landauer-Büttiker formula [17].

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I_{ds}(V_d, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \left\{ T(E, V_d, V_g) [f_s(E - \mu_s) - f_d(E - \mu_d)] \right\} dE, (1)
\]

where T(E, Vd, Vg) represents the transmission coefficient, whereas fs(d) denotes the source (drain) Fermi-Dirac function. Additionally, \( \mu_{s(d)} \) indicates the Fermi potential for the source (drain). Specifically, the basis set that double ζ polarized is implemented. The exchange-correlation phenomenon is characterized by the utilization of a generalized gradient approximation inside the functional framework by Perdew Burke Ernzerh with the adoption of the model of a single electron [18]. Since doping carriers largely mask the electron-electron interaction, the model of a single electron is qualified to describe an electronic device’s structure [19, 20]. The k-point grids [21] are defined using the Monkhorst-Pack scheme as 9×9×1 and 9×9×175 for the central region and the electrode region within the Brillouin zone, respectively. The mesh cutoff established at 125 hartrees, while the temperature maintained at 300 K. To avoid interlayer interaction, a vacuum space of 10 Å is implemented as a boundary condition. The structure optimization process has been carried out until the energy difference per atom reaches 10^-6 eV. The boundary conditions are periodic in the x-direction, Neumann in the y-direction, and Dirchlet in the z-direction, as illustrated in fig. 1. The direction of transportation is aligned with the z-axis.

**Results and Discussion**

The construction of the GaNNT MOSFET model involves the utilization of intrinsic GaN material (Lch ≤ 5 nm) as the channel. The design setup depicted in Fig. 1 employs double gates, to utilize strongly n- or p-doped GaNNT as electrodes. The optimal doping concentrations for the electrodes are determined to be 4×10^{13} cm^{-2} for n doping and 6×10^{13} cm^{-2} for p doping, respectively, as per the results of the test. Gate lengths were set to range from 1 to 5 nm, in 1 nm step with SiO2, HfSiO4, HfO2, La2O3, and TiO2 as the oxide dielectric material. The range for the oxide thickness is established to be between 0.1 and 0.5 nm, with increments of 1 nm, and the supply voltage (Vdd = Vb = 0.5 V) is adopted for each device.

![Fig. 1. Schematic view of DG GaNNT MOSFETs.](image)

The l_on and l_off parameters are crucial metrics for evaluating the performance of logic transistors. A lower l_off value signifies lower static power dissipation, while a higher l_on value indicates enhanced operational speed of the device. The values of l_on in n-type MOSFETs are achieved by measuring the Vg(on) = Vg(off) + Vdd, conversely. The l_off values for p-type MOSFETs are typically determined at the Vg(on) = Vg(off) − Vdd. Here, the Vg(off) for all devices is zero. Fig. 2 (a and b) illustrates the transfer features of the n-type and p-type DG GaNNT FETs with the Lch sub-5 nm for different gate lengths, oxide dielectric material, and oxide thickness by adjusting the gate voltage within the range of 0 to 1 V at supply voltage Vdd = Vb = 0.5 V.
$I_{ds}$ curves of n and p-type FETs at $L_g = 5$ nm with EOT=0.1 nm show increased $I_{th}$ with higher gate dielectric materials, as represented in fig. 2 (c and d). In these figures, the $I_{ds}$ exhibits a greater magnitude when considering TiO$_2$ as compared to other dielectric materials. An increase in the dielectric constant leads to an increase in the gate capacitance, thereby resulting in an increase in the inversion charge. An elevation in the inversion charge leads to a corresponding augmentation in the $I_{ds}$ due to the Low conduction band edge energy of FETs with a high dielectric material[22], implying that the process of conduction takes place at reduced energy levels, which makes the TiO$_2$ and La$_2$O$_3$ materials are better candidates as gate dielectric. At $L_g = 5$ nm and SiO$_2$ dielectric layer, fig.2(e and f) shows the decrease of driving current for the same gate voltage due to an increase in oxide thickness which leads to the reduction of gate capacitance[23].

The $I_{on}/I_{off}$ ratio serves as a key metric for evaluating the performance of a device, as it reflects the ability to achieve high performance (large $I_{on}$ value) while minimising leakage power (small $I_{off}$ value). In this context, the value of $I_{on}$ is determined when the $V_g$ is equal to the threshold voltage ($V_{th}$), while the value of $I_{off}$ is determined when $V_g$ is set to 0 V. According to fig. 3 (a), it can be observed that there is an increase in the $I_{on}/I_{off}$ ratio as the $L_g$ is increased. The $I_{on}/I_{off}$ ratio exhibits an increase as the $L_g$ is extended, because the $I_{on}$ experiences an increase while the $I_{off}$ undergoes a drop. Moreover, it can be observed from fig. 3 (b) that the $I_{on}/I_{off}$ ratio exhibits an upward trend as the dielectric constant increases. In a similar vein, it can be observed from fig. 3(c) that there is a notable decrease in the $I_{on}/I_{off}$ ratio as the $t_{ox}$ is increased.


(a) gate lengths, (b) oxide dielectric material, and (c) oxide thickness.

In order to assess the effectiveness of gate control, the SS holds significant importance [24]. Enhanced gate control is correlated with a reduced SS in subthreshold region. Based on the formula $SS = \frac{\partial V_g}{\partial \log I_{ds}}$ [25], the term SS represents the magnitude of the change in $V_g$ required to induce a 1 dec alteration in the current. According to the references [26, 27], it is widely believed that long channel conventional MOSFETs, which typically have dimensions in the micrometer range, exhibit a fundamental SS limit of 60 mV/dec at ambient temperature. As depicted in fig. 4 (a), the SS values of the GaNNT MOSFETs exhibit a decreasing trend as the $L_g$ increases. Notably, the SS value experiences a significant reduction from 95 to 78 mV/dec when $L_g$ increases from 1 to 5 nm. The reduction of leakage from the source to the drain is achieved by raising the dielectric constant. This, in turn, effectively lowers the SS to 62 mV/dec when utilizing TiO$_2$ as the dielectric material, as depicted in fig. 4 (b). The value of SS exhibits a progressive increase as the $t_{ox}$ increases, eventually reaching a value of 98 mV/dec at a thickness of 0.5 nm, as depicted in fig. 4 (c).

Transconductance an additional significant element, plays a role in regulating the behaviour of the gate inside the subthreshold region. This can be expressed as the derivative of drain current with respect to gate voltage, denoted as ($g_m = \frac{\partial I_{ds}}{\partial V_g}$) [24]. A greater value of $g_m$ is expected to enhance the capacity to control gates. Generally, the parameter $g_m$ exhibits an upward trend as both $L_g$ and the dielectric constant increase, as depicted in fig. 5 (a, b). Conversely, $g_m$ experiences a decline when $t_{ox}$ grows, as illustrated in fig. 5 (c).

Fig.4. Subthreshold swing of DG GaNNT MOSFETs as a function of (a) $L_g$, (b) oxide dielectric material, and (c) $t_{ox}$.

Fig.5. Transconductance of DG SWAlNNT MOSFETs with $L_g$. 

[4]
(a), oxide dielectric material (b), and t_ox (c).

The characteristic of digital circuits is determined by their switching speed. The calculation of switching speed involves the utilization of the formula \( \tau = C_t V_{dd} / I_{on} \) \([28]\). In this equation, \( C_t \) represents the total capacitance, which is the combination of fringing capacitances (\( C_f \)) and channel capacitance (\( C_{ch} \)) \([24]\). The determination of \( C_{ch} \) can be accomplished by employing the formula \( C_{ch} = \partial Q_{ch} / \partial V_g \), where \( Q_{ch} \) denotes the total Mulliken charge of the central region and \( W \) represents the channel width. Based on the reference provided \([24]\), it is assumed that the value of \( C_{ch} \), the channel capacitance, is twice that of \( C_i \), the intrinsic channel capacitance. In general, it can be observed from fig. 6 (a, b) that the parameter \( \tau \) demonstrates a decreasing pattern with increasing values of \( L_g \) and the dielectric constant. In contrast, the variable \( \tau \) exhibits an upward trend as the parameter \( t_ox \) increases, as depicted in fig. 6 (c).

![Fig.6. Delay time of DG GaNNT MOSFETs with \( L_g \) (a), oxide dielectric material (b), and \( t_{ox} \) (c).](image)

In the context of MOSFET applications, the PDP, denoted as \( PDP = V_{dd} I_{on} \tau \), serves as a significant metric for evaluating the switching energy for digital circuits. In fig. 7, an analysis was conducted on the power-delay product (PDP) of 2D-channel GaNNT MOSFETs for both n-type and p-type. The results indicate that the PDP exhibits a little drop as the \( L_g \) and dielectric constant increase, as shown in fig. 7(a and b). whereas, it increases with the \( t_{ox} \), as depicted in fig. 7(c).

![Fig.7. PDP of DG GaNNT MOSFETs with \( L_g \) (a), oxide dielectric material (b), and \( t_{ox} \) (c).](image)
Conclusion
The performance of GaNNT MOSFETs, both n-type and p-type MOSFETs, has been examined using the ab-initio DFT technique. This investigation focused on the influence of gate length, oxide dielectric material, and oxide thickness. The simulation findings demonstrate that the $l_{on}/l_{off}$ ratio can be significantly enhanced by increasing the gate length and dielectric constant, as well as by decreasing the oxide thickness. For SS, the results indicate a notable enhancement in mitigating short channel effects as the gate length extended to 5 nm. In the context of τ and PDP, it has been discovered that there is a notable enhancement in the short channel impact at the gate length increased, the dielectric constant is increased, and the oxide thickness is decreased. This improvement is particularly prominent when considering a channel length of 5 nm for n-type devices. Therefore, GaNNT exhibits considerable promise as a channel material for the development of complementary MOSFETs suitable for both n-type and p-type devices.

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Conflict of Interest
The author declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethical Statement
Hereby, the following is fulfilled:
1) This material is the authors’ own original work, which has not been previously published elsewhere.
2) The paper is not currently being considered for publication elsewhere.
3) The paper reflects the authors' own research and analysis in a truthful and complete manner.
4) The paper properly credits the meaningful contributions of co-authors and co-researchers.
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